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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,237	08/27/2003	Chaur-Chin Yang	BHT-3183-53	3764

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BRUCE H. TROXELL
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EXAMINER

ROSE, KIESHA L

ART UNIT PAPER NUMBER

2822

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/648,237	YANG ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 December 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 25-38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 25-38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the amendment filed 20 December 2004.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 25-28,33-34 and 36-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Giri et al. (U.S. Patent 6,765,152).

Giri discloses a chip module (Figs. 1-4) that contain a substrate (12) (printed circuit board) having a top surface, bottom surface and a substrate opening extending through the top surface and the bottom surface, a dummy die (18) connected to the bottom surface and aligned with the substrate opening, wherein the dummy die has a redistribution layer electrically connected with the substrate having flip chip pads and connecting pads connected by a trace on the top surface of the dummy die, a chip (22) located in the opening and having a plurality of bumps electrically connected with the flip chip pads of the redistribution layer where the dummy die is larger than the chip, packaging (34) located in the substrate opening and encasing the chip, a plurality of top

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connection pads located on the top substrate surface, solder balls (14) formed on the bottom surface of the substrate and the dummy die has an exposed surface located on the bottom surface and has a metal thermal conducting layer (layer on the underside of the dummy die where the other chips are formed) and adhesive tape can be used to connect the dummy die to the bottom substrate surface. (Fig. 3)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 29-30 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giri in view of Klein et al. (U.S. Publication 2004/0145051).

Giri discloses all the limitations except for stacked semiconductor package and pitch size for the flip chip pads. Whereas Klein discloses a semiconductor package (Fig. 9a) that contains a die (12) with a redistribution layer formed thereon with flip chip pads (22) and connecting pads where the flip chip pads have a smaller pitch than the connecting pads and a plurality of stacked semiconductor packages including a plurality of outer terminals (118) connecting the connection pads (52). The package is a stacked semiconductor package in order to form a system. (Page 7, Paragraph 96) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Giri by incorporating a stacked semiconductor

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package to create a system for electrical connection as taught by Klein. In regards to claims 29 and 30, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the pitch of the flip chip being 150 μ m, since it has been held that discovering the optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (1980).

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Giri in view of Kikuma et al. (U.S. Patent 6,621,169).

Giri discloses all the claimed limitations except for bonding wires connecting the redistribution layer to the substrate. Whereas Kikuma discloses a stacked semiconductor device (Fig. 25) that contains a substrate (108) and a chip with a redistribution layer (114) formed thereon where the redistribution layer and substrate are connected by bonding wires (116). The substrate and redistribution layer are connected by bonding wires to form an electrical connection between the two. (Column 17, lines 60-64) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Giri by incorporating the redistribution layer and substrate to be connected by bonding wires to form an electrical connection between the two as taught by Kikuma.

Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Giri in view of Koopmans (U.S. Publications 2004/0035840).

Giri discloses all the limitations except for bumps bonding the connecting pads of the redistribution layer to the substrate. Whereas Koopmans discloses a flip chip (Fig. 1a) that contains a substrate (34) and a redistribution layer (21) with connecting pads

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(20) and bumps (26) that bond the connecting pads of the redistribution layer to the substrate. The bumps are formed between the connecting pads of the redistribution layer and the substrate to enable electrical interconnection to a package (redistribution layer and substrate). (Page 1, Paragraph 7) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Giri by incorporating bumps between the connecting pads of the redistribution layer and the substrate to enable electrical interconnection to a package (redistribution layer and substrate) as taught by Koopmans.

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Giri in view of Higgins III (U.S. Patent 5,583,377).

Giri discloses all the claimed limitations except for the substrate to have a stair configuration. Whereas Higgins discloses a semiconductor device (Fig. 2) that contains a substrate (42) with a stair configuration (44) and a chip (13) mounted in the opening of the substrate. The substrate is formed with a stair configuration to help with the manufacturing cost and form a lower profile device. (Column 5, lines 18-20) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Giri by incorporating the substrate to have a stair configuration to help with manufacturing cost and make a lower profile device as taught by Higgins.

Response to Arguments

Applicant's arguments with respect to claims 25-38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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